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CMOS Readout Circuit Developments for Ion Sensitive Field Effect Transistor Based Sensor Applications

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1. Introduction

Biomimetic devices have become more and more important in modern life where populations are aging; and the applications of electronic tongue system to water quality and environmental monitoring have become a significant field all over the world. Electronic tongue system uses sensor arrays and signal processing techniques such as identification, classification and recognition for quantitative multi-component analysis and for artificial assessment of taste and flavor of various liquids (Cjosek & Wroblewsk, 2007). Ion Sensitive Field Effect Transistor (ISFET), an electrochemical and potential type sensor, has served as excellent candidate for various electronic tongue applications.

The ISFET, invented by Bergveld in 1970, is a solid-state device that combines a chemically sensitive membrane with a MOS type field-effect transistor (Bergveld, 1970). Due to its small size, rapid pH response and rugged solid-state construction, the ISFET exhibits a number of advantages over conventional pH-glass electrodes. ISFET has been extensively studied in past 36 years (Bergveld, 1991 and 2003; Garde et al., 1995). The current status and trends of main ISFET-based research, shown in Fig.1, are (1) single and sensor array applications, (2) ISFET micro-system fabrication in a standard CMOS technology, and (3) diversified ISFET-based biosensor development. For example, the ISFET research topics in Taiwan for the past ten years (Yin et al., 2001; Chin et al., 2001; Chung et al., 2004, and 2008) are focused on the study of new sensing material, on fabrication technology and device structure development, on diversified field applications, on the study and improvement for non-ideal characteristics, and on new readout circuit development. Based on our previous researches, the key problems in readout circuit development are due to the inherent characteristics of ISFET and to the body effect caused by common substrate of sensor array applications. The inherent characteristics of ISFET, like time drift and temperature dependency, cause

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drawbacks on ISFET continuous-mode monitoring applications. Furthermore, the conventional floating-source constant-voltage and constant-current circuit (Caras & Janata, 1980) in Fig. 2 faces problems including noise interference, requirement of two external current sources and body effect. In order to solve the aforementioned problems, this chapter focuses on developing a series of improved readout circuit techniques that enhances the performance of ISFET and demonstrates their pH sensing capability for environmental monitoring.

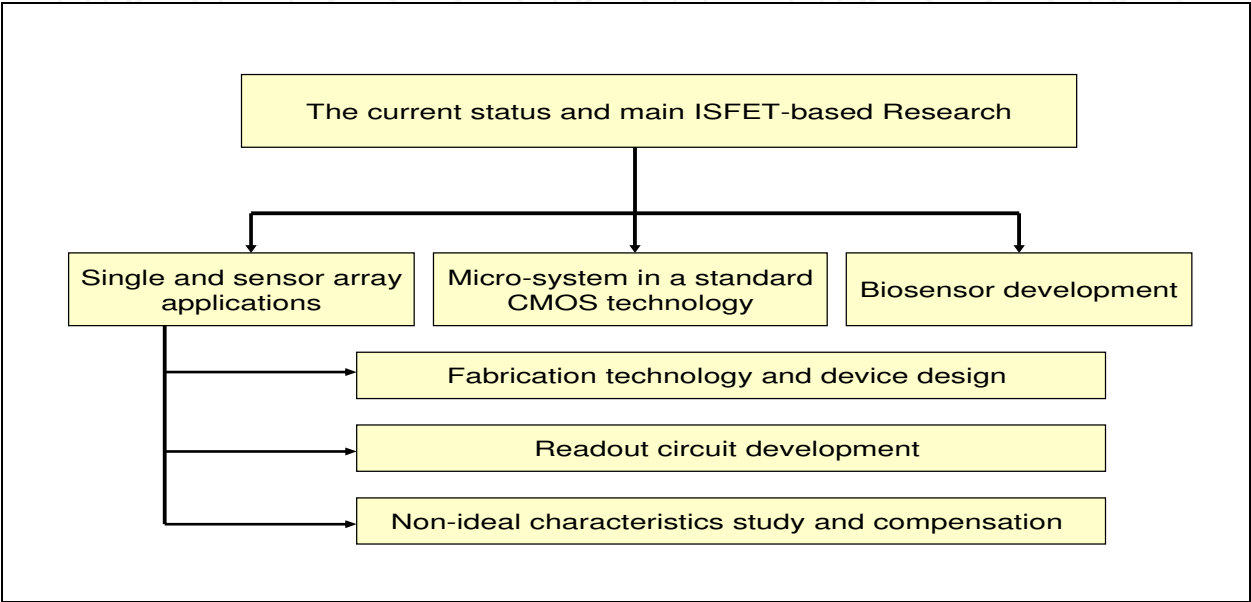


Fig. 1. The current status and main ISFET-based research

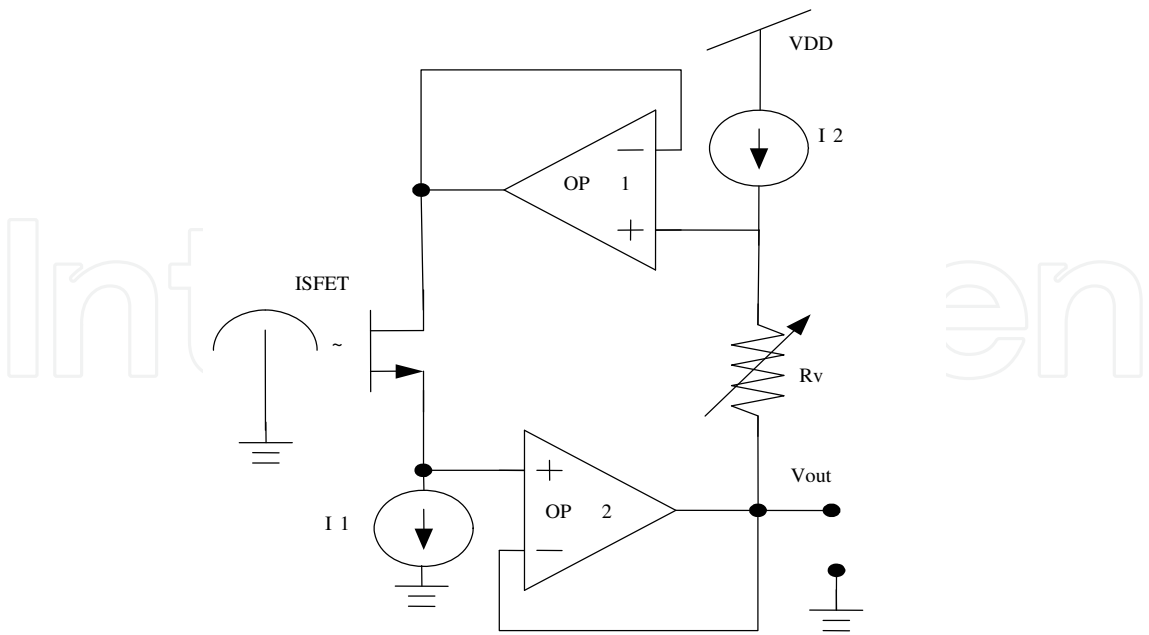


Fig. 2. A conventional floating source constant-voltage constant-current circuit (Caras & Janata, 1980)

Section 2 of this chapter explores the main concerns on ISFET device structure, operation and its stable signal readout circuit design. A bridge-type floating source circuit is developed for ISFET-based single and sensor array applications.

In order to investigate the performance of readout circuit due to the non-ideal characteristics of ISFET such as drift response, **Section 3** develops a behavioral macro model for a depletion-mode ISFET with a silicon nitride gate insulator.

Fig. 3 gives a typical measured data for Si_3N_4 -gate ISFET at different pH buffer solutions. The temperature dependency may cause around 15% error in pH reading in real applications. **Section 4** demonstrates and investigates a V_{TH} extractor circuit that provides sensitive measurements with improved temperature compensation. This circuit uses Si_3N_4 -gate ISFET and depletion-type MOSFET sensor pairs that are fabricated on the same wafer.

Section 5 develops a new readout circuit that improves the performance parameters, including stability of readout circuit, dependency of temperature, and wide-usage for sensor array applications. A bridge-type floating source circuit with body-effect reduction has been developed for capturing more accurate threshold voltage variation which is corresponding to different H^+ concentrations. The presented readout circuit interface improves the accuracy of pH measurements, while maintaining operation at constant drain-source voltage and current condition.

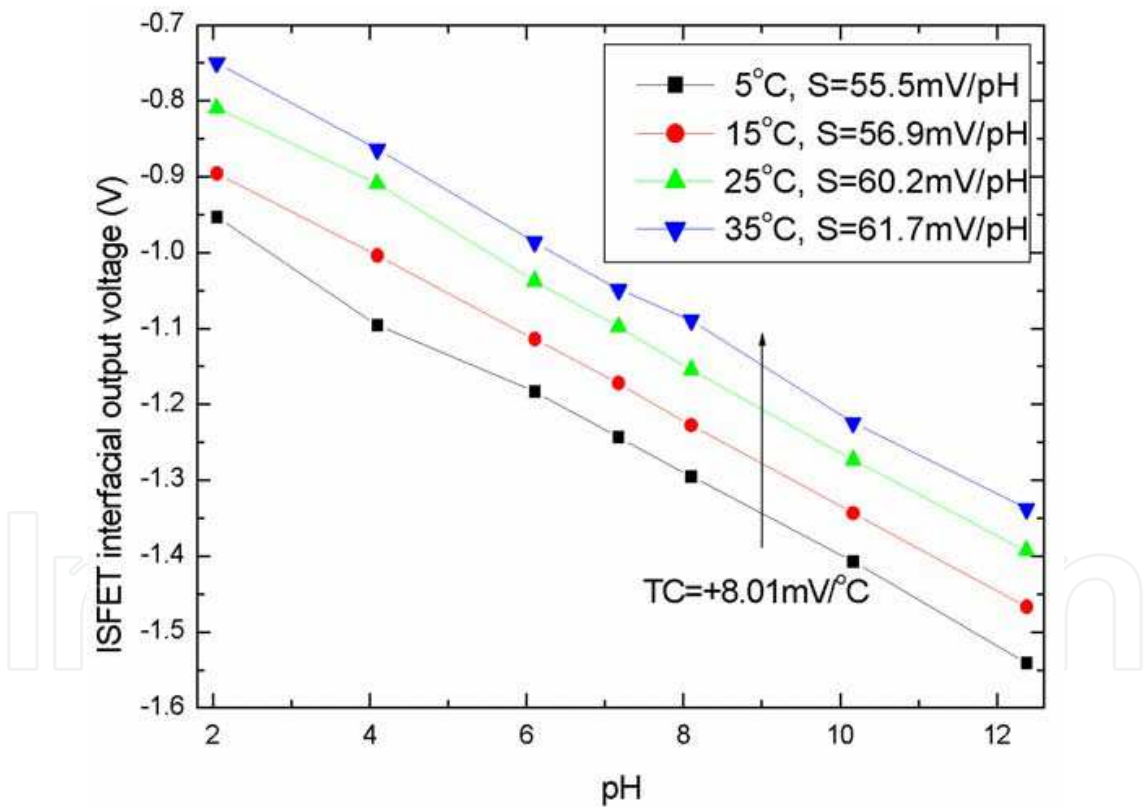


Fig. 3. Measured data versus different pH buffer solution with temperature variation.

2. ISFET operation and its signal readout

ISFET-based potentiometric transducers have created valuable applications in biomedical data acquisition and environmental monitoring. Two basic Si_3N_4 -gate ISFETs are depicted in Fig. 4. In Fig. 4(a) is a simple ISFET device structure that is compatible to a standard p-

substrate CMOS process, while in Fig. 4(b) is an n-substrate/p-well/n-type ISFET which have a better performance in sensor array application because of isolated p-well structure.

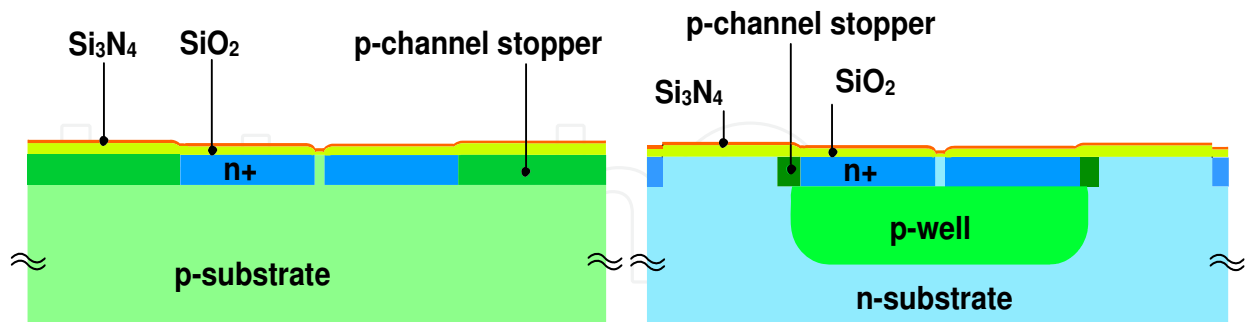


Fig. 4. (a) p-substrate/n-type ISFET; (b) n-substrate/p-well/n-type ISFET

The model of a conventional MOSFET device can also define an ISFET sensor (Bergveld, 1970) as in (2.1). The only difference is that the threshold voltage of MOSFET is replaced by the threshold voltage of ISFET.

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH(ISFET)}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (2.1)$$

The I_{DS} is drain current, μ_n is mobility of electron carriers in semiconductor layer, C_{ox} is oxide capacitance density, W/L is device aspect ratio, V_{GS} is gate-source voltage, V_{DS} is drain-source voltage, and $V_{TH(ISFET)}$ is the threshold voltage of ISFET.

With gate region exposed to the chemical solution, the threshold voltage of ISFET changes accordingly with the activity of ions in the chemical solution. This electrochemical phenomenon is defined by Nernst for single-ion, e.g., hydrogen in (2.2) and (2.3).

$$V_{TH(ISFET)} = V_{TH(MOSFET)} - V_{CHEMICAL} \quad (2.2)$$

$$V_{CHEMICAL} = E_i + \frac{RT}{n_i F} \ln(a_i) \quad (2.3)$$

The $V_{TH(ISFET)}$ is a combined outcome of $V_{TH(MOSFET)}$ and $V_{CHEMICAL}$. The $V_{TH(MOSFET)}$ is threshold voltage of inherent MOSFET structure in ISFET, $V_{CHEMICAL}$ is electrochemically induced voltage in the threshold voltage of ISFET, E_i is chemical constant, R is gas constant, T is absolute temperature in Kelvin, F is Faraday constant, n_i is charge of ion i , and a_i is ion activity of ion i . To include the effect of ion activity to ISFET electrical characteristics, the Nernst model is added to the ISFET equation as in (2.4).

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} V_{DS} \left[V_{GS} - V_{TH(MOSFET)} + \left[E_i + \frac{RT}{n_i F} \ln(a_i) \right] - \frac{1}{2} V_{DS} \right] \quad (2.4)$$

When ISFET is connected to a readout circuit, the output voltage V_{OUT} is usually the gate-source voltage V_{GS} of ISFET. From (2.5), the V_{GS} of ISFET is proportional to the logarithmic function of ion activity a_i . Hence, the V_{OUT} of readout circuit reflects the ion activity.

$$V_{GS} = \frac{I_{DS}}{\mu_n C_{ox} \frac{W}{L} V_{DS}} + V_{TH(MOSFET)} - E_i - \frac{RT}{n_i F} \ln(a_i) + \frac{1}{2} V_{DS}$$

(2.5)

In order to monitor the change of ion activity, ISFET should operate in the linear region ($V_{DS} < V_{GS} - V_{TH}$) and should maintain constant voltage constant current mode (CVCC). These conditions make the gate-source voltage (V_{GS}) proportional to the internal threshold voltage. We developed a more stable bridge-type readout circuit for ISFET pH sensor, shown in Fig.5. This circuit provides low drain-source voltage (V_{DS}) to ensure the linear operating condition of ISFET and maintain CVCC mode ($V_{DS} = 0.5V$, $I_{DS} = 100\mu A$) so that the gate-source voltage, which is the output voltage (OUT) of the circuit, becomes proportional to the threshold voltage of ISFET. Hence, the output voltage also becomes proportional with the pH concentration of solution. Equations (2.6) to (2.8) show the basic concept of circuit operation, where V_1 is a voltage drop across R_1 and R_2 .

$$V_{DS} = V_{R2} = V_1 \left[\frac{R_2}{R_1 + R_2} \right]$$

(2.6)

$$I_{DS} = I_{R3} = \frac{V_1 - V_{DS}}{R_3}$$

(2.7)

$$\begin{aligned} OUT &= V_{GS} = f(V_{TH(ISFET)}) = f(pH) \\ OUT &= V_{RE} - V_{OUT}; V_{RE} = 0V = grounded \\ OUT &= -V_{OUT} \end{aligned}$$

(2.8)

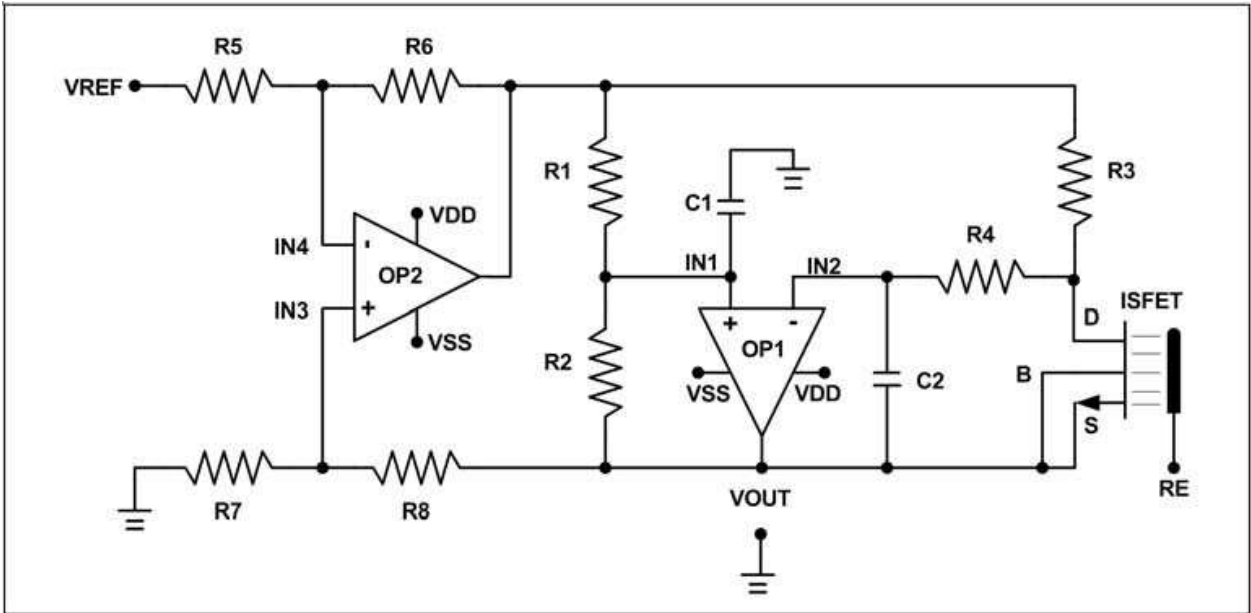


Fig. 5. The schematic diagram of ISFET bridge-type readout circuit

To enhance the signal to noise ratio, the readout circuit incorporated two low pass filters (LPF) for removing noise signals from the power supply and the ISFET itself, namely from the external electromagnetic field interference or the fluid fluctuation. One LPF is formed by

R_1 , R_2 and C_1 , and the other LPF is provided by R_3 , R_4 , R_{DS} and C_2 . The pass band edge f_p is set by (2.9):

$$f_p = \frac{1}{2\pi(R_4 + R_3 \parallel R_{DS})C_2} = \frac{1}{2\pi(R_1 \parallel R_2)C_1} \quad (2.9)$$

The ISFET bridge-type readout circuit shown in Fig. 5 can be extended for sensor array applications. Instead of using a single ISFET sensor, a parallel configuration of ISFET sensors with respective analogue switches in each leg has been designed as in Fig. 6. The key concern of this design is the response time and linearity of analogue switches.

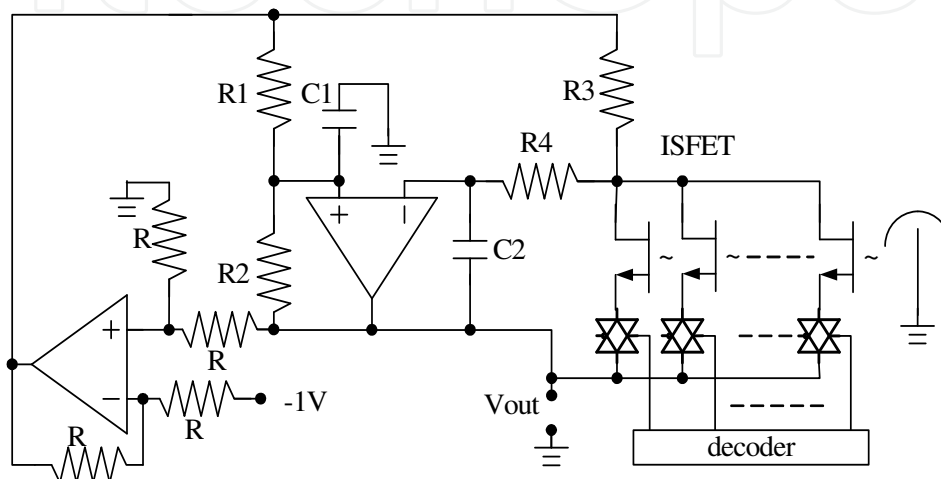


Fig. 6. The schematic diagram of bridge-type readout circuit for ISFET sensor arrays

3. Modelling the ISFET drift effects

For long-term monitoring, the drift effect of ISFET sensor is frequently observed which can last up to several hours. Studies have indicated that a drift effect of ISFET limits the measurement accuracy and quality of water monitoring.

Electronic circuit simulation programs such as SPICE (Simulation Program with Integrated-Circuit Emphasis), which were originally developed for designing and simulating electronic circuits, can also be adapted to design silicon-based chemical- and bio-sensors micro-system. Researches to model the ISFET was carried out in two main ways: (a) development of physical-chemical models (Jamasb et al., 2000; Kuhnhold et al., 2000; Chou et al., 2000) and (b) investigation of electronic circuits by SPICE built-in models or macro models (Martinoia et al., 1999; Lauwers et al., 2001). In order to include the drift effect of ISFET for circuit simulation, we developed a behaviour model which can be used in circuit design using SPICE simulator.

3.1 Drift effect of ISFET

Based on the CVCC and constant temperature conditions, ISFET drift is defined as the shift of dV_{GS}/dt . Previous works reported that the non-ideal effects of the ISFET are modelled by both responses of buried sites and the surface oxidation of silicon nitride (Bousse et al., 1990; Kuhnhold et al., 2000). The sensor output signal is influenced by both fast and slow responses. The fast time dependence is caused by the surface oxidation of silicon nitride,

while the response due to buried sites mainly affects the slow pH response. So, the effective ISFET threshold voltage, V_{TH}^* , is given with time dependence by equation (3.1) (Liao, 2000):

$$V_{TH}^* = V_{TH}(0) + \Delta V_{THFS}(t) + \Delta V_{TDFT}(t) \quad (3.1)$$

Where $V_{TH}(0)$ is the original threshold voltage of ISFET at time $t=0$, $\Delta V_{THFS}(t)$ is the contribution of the drift effect by fast and slow responses, and $\Delta V_{TDFT}(t)$ is the drift-induced threshold voltage variation during the overall time interval of interest. The $\Delta V_{THFS}(t)$ can be expressed as (3.2):

$$\Delta V_{THFS}(t) = fm \times (1 - e^{-t/\tau_f}) + sm \times (1 - e^{-t/\tau_s}) \quad (3.2)$$

Where fm is the maximum shift of threshold voltage due to the fast time response, sm is the maximum shift of threshold voltage caused by the slow time response, τ_f and τ_s are the time constants of fast and slow responses. The typical values for τ_f and τ_s are several seconds and 2 to 3 hours, respectively. In addition, the $\Delta V_{TDFT}(t)$ can be modeled by (3.3):

$$\Delta V_{TDFT}(t) = dm \times (1 - e^{-t/\tau_{ov}}) \quad (3.3)$$

Where τ_{ov} is the time constant of overall time interval of interest, and dm is the maximum drift during a long period of measurement. The drift rate can be defined by (3.4):

$$\text{Drift rate} = \frac{d\Delta V_{TDFT}(t)}{dt} = \frac{dm}{\tau_{ov}} e^{-t/\tau_{ov}} \quad (3.4)$$

Thereby, a constant drift rate of dm/τ_{ov} and a drift rate of 0 mV/hour can be given for $t \ll \tau$ and $t \rightarrow \infty$, respectively. From equations (3.1) to (3.4), the overall drift-induced threshold voltage variation can be concluded in (3.5):

$$\Delta V_{T_{overall}} = fm \times [1 - \exp(-\frac{t_f}{\tau_f})] + sm \times [1 - \exp(-\frac{t_s}{\tau_s})] + dm \times [1 - \exp(-\frac{t_d}{\tau_{ov}})] \quad (3.5)$$

In 2000, Chou et al. reported that the drift rate increases as the temperature rises (Chou et al., 2000) according to the following relation in (3.6):

$$\Delta V_{d,Temp} = c_{T1} \times \exp(-\frac{c_{T2}}{T}) \quad (3.6)$$

Where T is the operating temperature, C_{T1} and C_{T2} are the coefficients of drift rate against temperature for different sensors. The ratio of operating temperature T to room temperature, i.e., 25°C is described in (3.7), where $driftT$ is the drift due to temperature variation.

$$driftT = \Delta V_{T_{overall}} \times \exp(-\frac{(25-T) \times c_{T2}}{25 \times T}) \quad (3.7)$$

In addition, drift rate is linearly proportional to pH value as described in (3.8):

$$\Delta V_{d,pH} = c_{pH} \times pH \quad (3.8)$$

Where c_{pH} is the coefficient of drift rate versus pH for different sensors; the ratio of pH to pH7 is described as (3.9)

$$drift_{pH} = \Delta V_{T_{Overall}} \times \left(1 - \frac{c_{pH} \times (7 - pH)}{drift_7}\right) \quad (3.9)$$

Where $drift_{pH}$ is the drift rate that changes with pH, and $drift_7$ is the drift rate at pH7. Finally, considering the dependence on temperature and pH value, the expression for the drift rate is provided in (3.10):

$$\Delta V_{TH,Temp,pH}^* = \Delta V_{TH_{Overall}} \times \left[1 - \frac{c_{pH} \times (7 - pH)}{drift_{pH7,25C}}\right] \times \exp\left\{-\left[\frac{(25 - T)}{25T} c_{T2}\right]\right\} \quad (3.10)$$

Where $\Delta V_{TH_{Overall}}$ is the drift rate at pH=7 and 25°C.

This study evaluated the n-channel p-well depletion-mode Si_3N_4 -gate ISFET sensor with $W/L=600\mu m/15\mu m$ and fabricated by the Institute of Electron Technology, Poland. The physical layout of this ISFET is provided in Fig. 7(a). Previous research (Martinoia & Massobrio, 2000) together with the approach we have formulated in equation (3.10), leads to the ISFET equivalent circuit shown in Fig. 7(b). The E_{ref} is the potential of reference electrode, C_{Gouy} and C_{Helm} are the Gouy-Chapman and Helmholtz capacitances, and E_{drift} models the drift response. The HSPICE-compatible macro model in Fig. 7(b) and Fig. 7(c) characterizes the ISFET as two stages: an electronic stage and an electrochemical stage. The nodes 1, D, S, and B stand for the reference electrode, drain, source, and bulk connections, respectively.

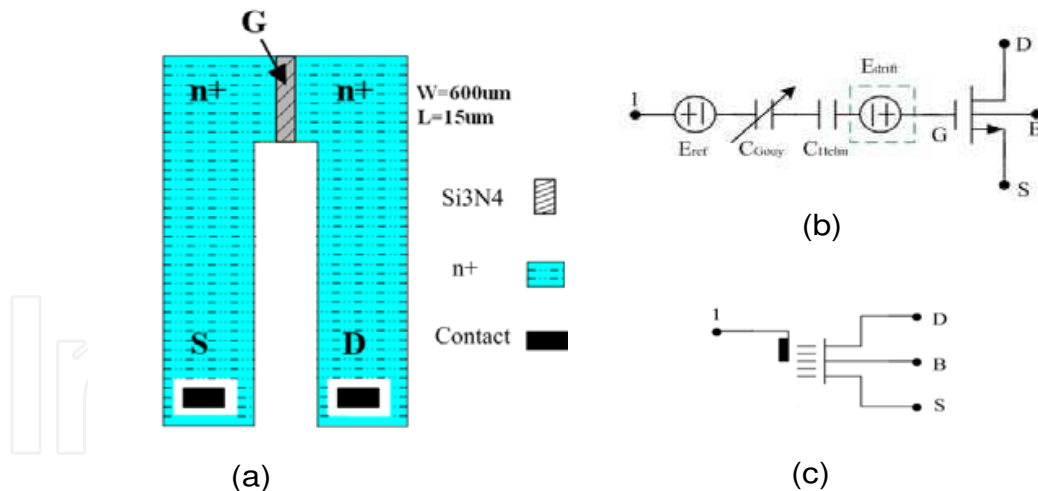


Fig. 7. (a) Physical layout of ISFET sensor, (b) equivalent circuit of the ISFET including drift effect, (c) HSPICE-compatible macro model connections

3.2 Experimental set-up and results

Based on the physical layout of ISFET sensor in Fig. 7(a), the electrical drain and source contacts are not close to the actual transistor drain and source terminals. Thus, a significant internal series drain resistance, series source resistance, and parasitic capacitances have to be considered.

In the following simulations and experiments, the ISFET is biased on a constant drain-source voltage of 0.5V and a constant drain current of 100 μ A (CVCC). The simulations were investigated using the developed ISFET macro model with incorporated drift effect, and using the designed bridge-type readout circuit mentioned in **Section 2**. The experiments used the standard buffer solutions purchased from Riedel-de Haen (Germany) with pH levels from 2 to 12. The measurements were conducted in a temperature-controlled system illustrated in Fig. 8.

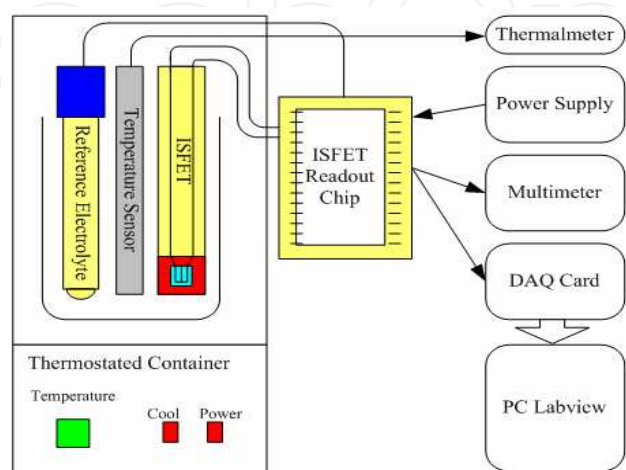


Fig. 8. Experimental set-up

The rail-to-rail op amp meets the design specifications to serve as a basic building block of the proposed bridge-type floating source readout circuit. The graph in Fig. 9 shows the dependence of ISFET source terminal potential over pH range of 2 to 12. The calculated slope for the curve is -46.34mV/pH and it presents a linear function with very high correlation coefficient of 0.998.

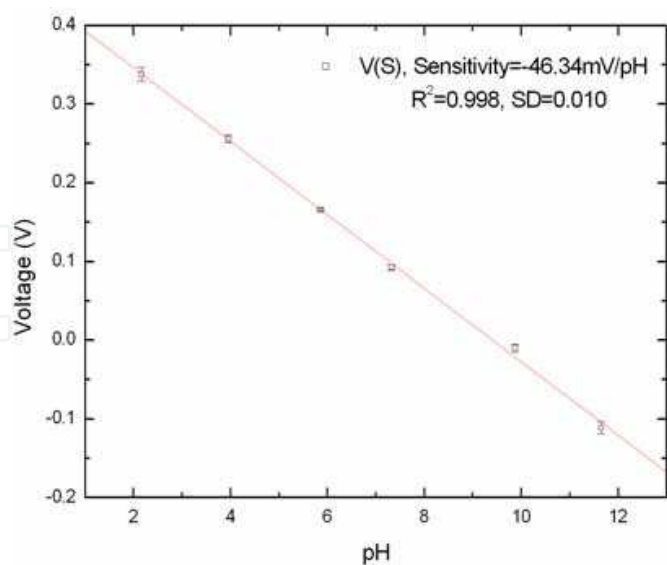


Fig. 9. ISFET readout voltage, VOUT in the pH range of 2 to 12

In order to evaluate the stability of the same ISFET sensor, the base line drift was measured twice using a standard buffer solution of pH 7. The drift rates of ISFET were evaluated after initial time of stabilization as a linear change of V_{GS} per time unit, and the drift rate is called

the drift coefficient, c_d (mV/hr). Fig. 10 shows the time response of ISFET for 18-hour time period operated in pH 7 at a controlled temperature of 25°C. The c_d values were calculated for experimental data after 4 hours of conditioning. The respective c_d for Test 1 and Test 2 are -1.44mV/hr and -1.34mV/hr with a standard deviation of 0.00838.

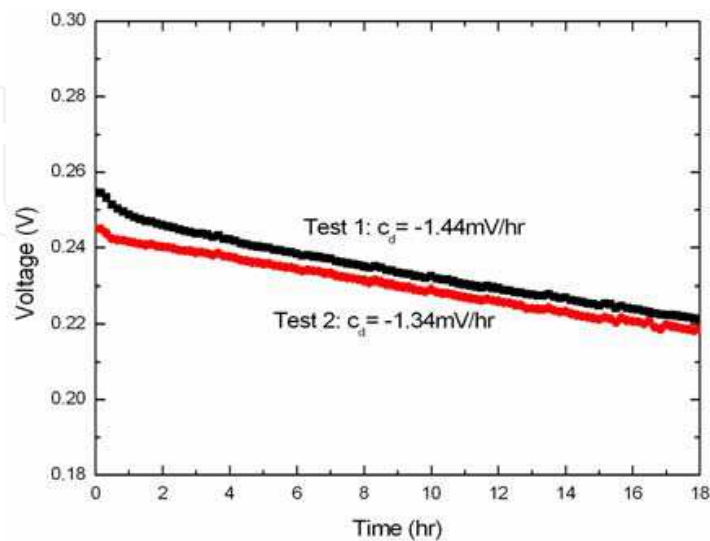


Fig. 10. The stability of ISFET in drift test

Like the time drift effect, the hysteresis also limits the accuracy of ISFET pH measurements. The hysteresis is a good marker to evaluate the reproducibility of the devices. In experiments, hysteresis tests are performed by titration in both direction, acidic or basic first and then in opposite direction to close the pH loop. Fig. 11 shows the time response of ISFET that was conditioned at pH 7 buffer solution and that went through titration with direction of pH 7→pH 12→pH 2→pH 7 in 10-minute step. Table 1 provides the parameter of Si_3N_4 -gate ISFET for a statistic group of 30 ISFET sensors. The width of hysteresis is the difference in the ISFET response at pH 6.0. The results present a good stability and good reproducibility of ISFET used. Based on the measurements, we conclude with the ISFET specifications in Table 2.

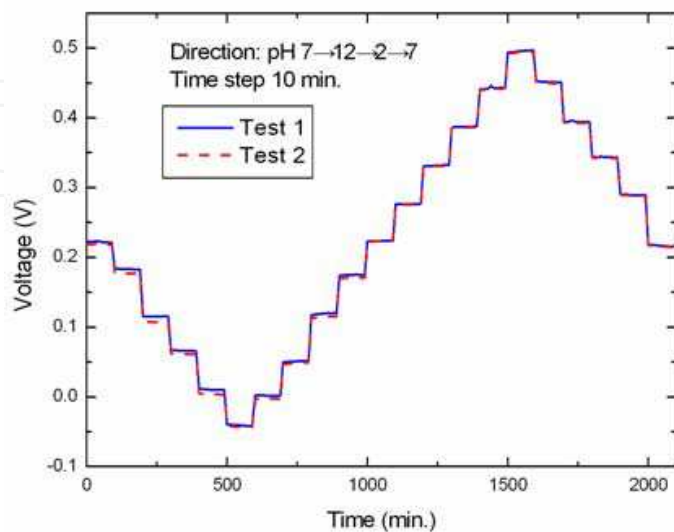


Fig. 11. Time response of reproducibility

Parameter	Range	Mean value	Standard deviation
Sensitivity (mV/pH)	-45.86~-47.12	-46.34	0.010
Correlation	0.996~0.9988	-	-
Drift (mV/hr)	-0.52~-1.71	-1.10	0.52
Hysteresis (mV)	9.22~13.0	11.1	2.68

Table 1. Parameter of Si₃N₄ gate ISFET

Item	Range
Bias condition	0.5V, 100μA
Temperature	5 ~40°C
Aspect ratio	600μm/15μm
Temperature coefficient	-0.9±0.5mV/°C
Drift coefficient	-1±0.5mV/hr
Hystersis	10±5mV
Sensitivity	-46±1mV/pH

Table 2. Specification of ISFET macro model

The ISFET drift data at room temperature was collected using the designed bridge-type readout circuit. The ISFET gate was applied using a commercial Ag/AgCl reference electrode immersed in a pH 7 buffer solution. Drift measurements and model parameter extraction were performed on a total of eight ISFET devices. The known and extracted parameters obtained on four devices, are given in Table 3. The modeled-versus-measured fit for an 18-hour time period depicted in Fig. 12 is characterized by an RMS error of 2.2%.

Parameter	Extracted value
<i>fm</i>	37.69mV
<i>sm</i>	33.28mV
<i>dm</i>	25.36mV
<i>C_{T2}</i>	60
<i>τ_f</i>	0.01 hour
<i>τ_s</i>	2 hour
<i>τ</i>	16 hour

Table 3. Extracted parameters for drift of Si₃N₄ ISFET

Dealing with the correlation of drift rate at different pH buffer solution, the measurement was done over a pH range of 2 to 12. The dependence of drift response on pH value between modeled and measured fit is shown in Fig. 13. The RMS error is 2.4%. The results show that the drift rate becomes larger as pH rises. Fig. 14 presents the measured drift rate at pH 7 as temperature varies from 5°C to 35°C. The temperature dependence on drift rate indicates an RMS error of 6.6% between modeled and measured fit.

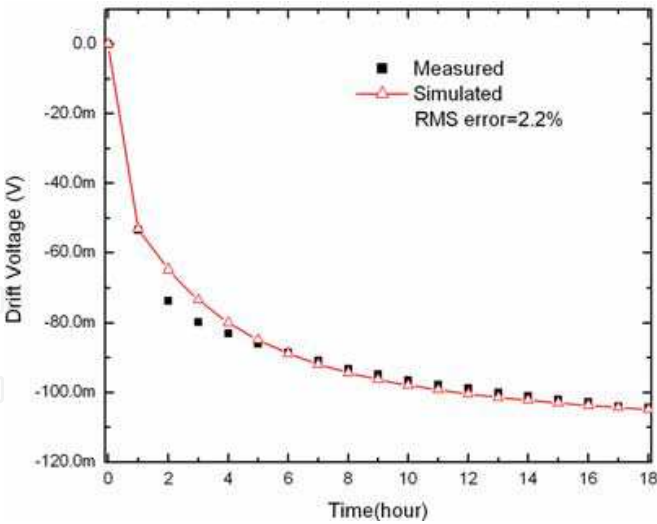


Fig. 12. ISFET drift characteristics at pH=7, 25°C

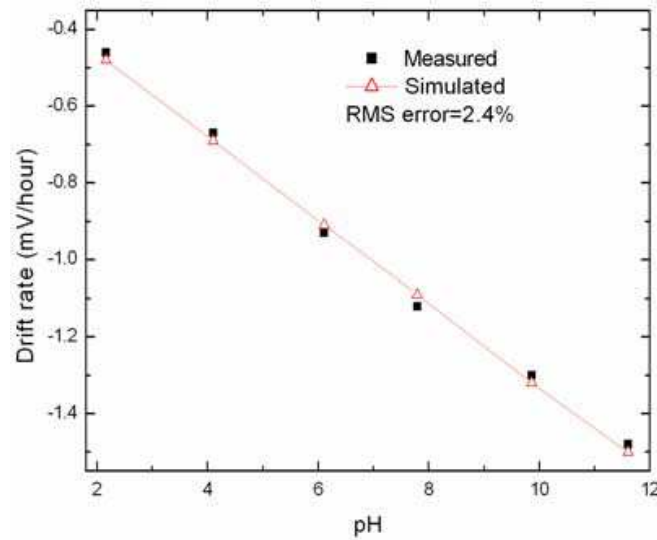


Fig. 13. Dependence of drift response on pH value

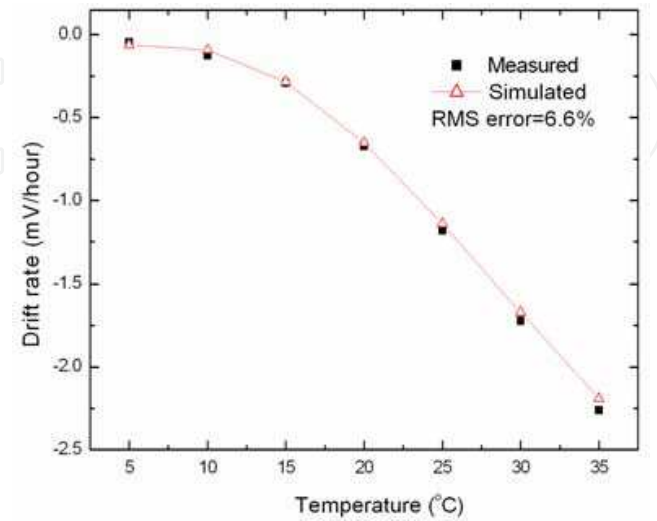


Fig. 14. Temperature dependence of drift rate

In conclusion, an HSPICE-compatible macro model that considers the drift response of pH ISFET has been presented. The modeled-versus-measured fit of the dependence of drift rate with long time period, temperature and pH variations present an RMS error of 2.2%, 2.4% and 6.6% respectively. The developed macro model can be adapted to speed up the design of silicon-based chemical- and bio-sensor micro-systems.

4. Temperature dependency of ISFET and its compensation

We developed a readout circuit that improved the performance of ISFET against non-ideal effects such as temperature dependency, time drift and hysteresis. The design concerns were also inspired by real application requirements for simpler and lower power consumption of the sensing system. Based on the concept of threshold voltage extractor (Wang, 1992), shown in Fig. 15, we developed a new ion sensing and interfacing circuitry with temperature compensation.

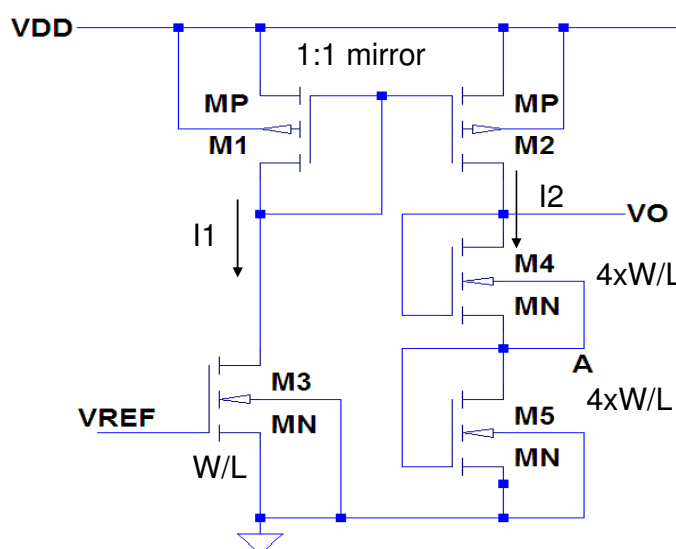


Fig. 15. Four-terminal extractor circuit (Wang, 1992)

With a 1:1 current mirror in M1 and M2, with specific W/L sizes of M3, M4 and M5, and with $I_{DM3} = I1 = I_{DM4} = I_{DM5} = I2$, the output voltage V_o of extractor circuit yields the threshold potential V_{TH} as expressed in equations (4.1) to (4.4).

$$I_{DM3} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{REF} - V_{TH})^2 \quad (4.1)$$

$$I_{DM4} = (4) \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(\frac{V_o}{2} - V_{TH} \right)^2 \quad (4.2)$$

$$\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{REF} - V_{TH})^2 = (4) \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(\frac{V_o}{2} - V_{TH} \right)^2 \quad (4.3)$$

$$V_o = V_{REF} - V_{TH} \quad (4.4)$$

Taking advantage of compatible CMOS process, the sensors that include ISFET and depletion-type Al-gate DMOSFET devices DM1 and DM2 were fabricated on the same wafer. Fig. 16 gives the complete design of a novel readout circuit of ISFET with temperature compensation based on the V_{TH} extractor circuits. It consists of blocks (a), (b), and (c). Block (a) is the ISFET pH sensing circuit. The gate and the drain of ISFET are connected together to make sure that it operates in saturation. The saturation drain-source current is set at $50\mu A$ because of the stable characteristics of ISFET in this value. With a fix drain-source current, the gate-source voltage of ISFET varies directly with its threshold voltage in the saturation region according to equation (4.1). As a result, the voltage V_{ISFET} is proportional with pH levels. However, the voltage V_{ISFET} exhibits temperature dependency with $V_{ISFET} = V_{pH} + V_{TEMP}$. Block (b) is the DMOSFET temperature sensing circuit. The voltage V_{TEMP} is proportional to the temperature value in DMOSFET. Block (c) is the output differential stage formed by M12 and M17 and served as subtractor circuit. The common temperature dependency of ISFET and DMOSFET is cancelled, and therefore the output voltage V_{COMP} is temperature compensated and is equal only to V_{pH} . Simulation results in Fig. 17(a) illustrate the voltage V_{ISFET} without temperature compensation and in Fig. 17(b) show the voltage V_{COMP} with temperature compensation.

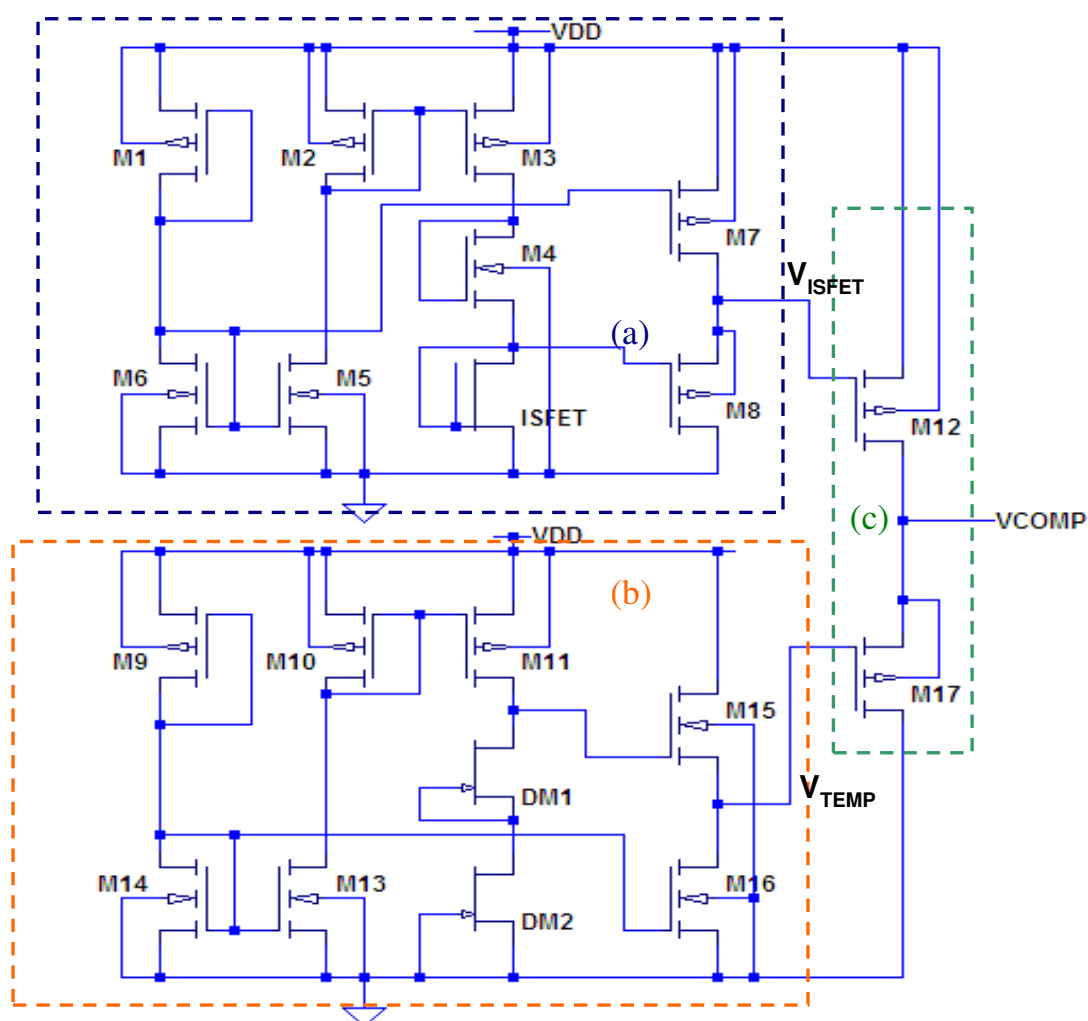


Fig. 16. V_{TH} extractor based readout circuit with temperature compensation

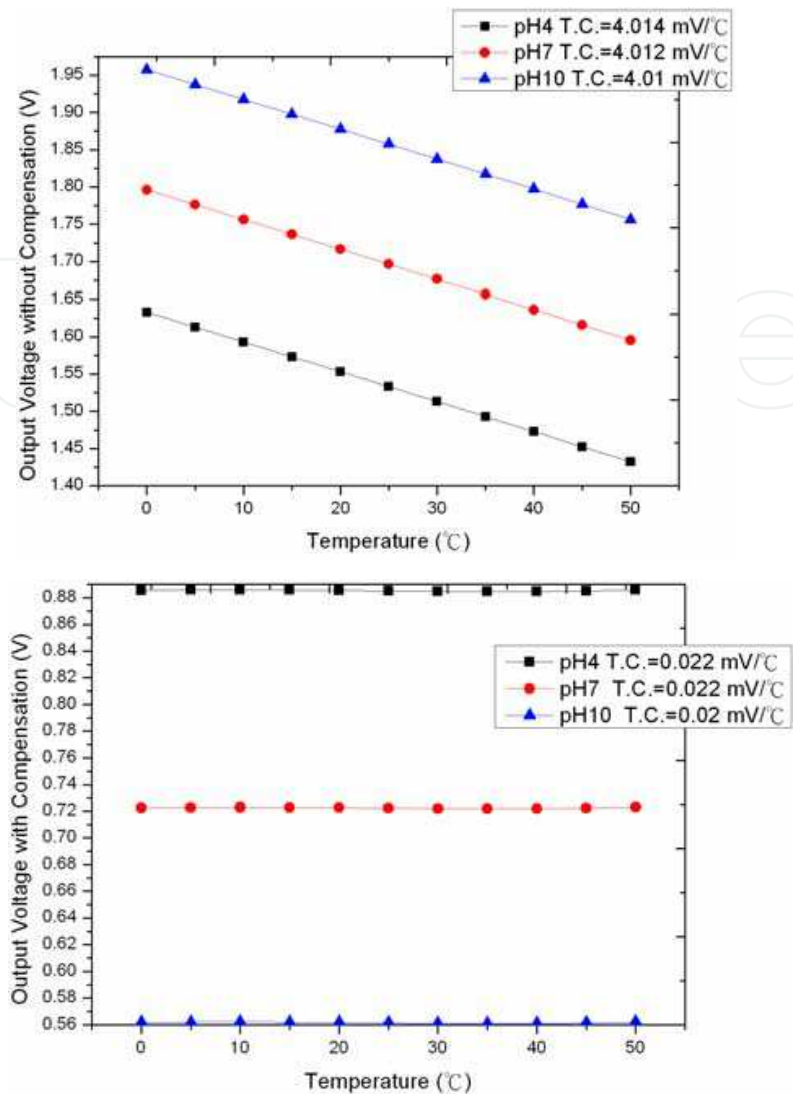


Fig. 17. (a) Output voltage without compensation, (b) output voltage with compensation

5. Body effect and its reduction technique

We have discussed the readout circuit techniques to improve the performance of ISFET over its inherent and non-ideal characteristics such as temperature-dependency and long-term time drift effects. To expand the benefits of most CMOS standard technologies, recent works have projected to integrate ISFET and interface electronics on the same chip (Wong & White, 1989; Ravczzi & Conci, 1998; Bausells et al, 1999; Palan et al, 1999; Chin et al, 2001). Because of low drift and high mobility properties of carriers, the n-channel ISFET devices are generally used. In most of current CMOS processes, the NMOS device is fabricated into a p-type substrate that is globally and constantly grounded to the most negative supply in the system. Thus, the above-mentioned interface circuits suffer from the problem where the substrate potential greatly influences the device characteristics in ISFET-based integrations. In 2004 Morgenshtein et al. presented a novel technique, which allows body effect elimination of readout interface in CMOS ISFET-based micro-systems (Morgenshtein et al, 2004). However, in this case a portion of the architecture of the ISFET does not have a constant current and voltage bias.

This section presents our approach of enhancing the accuracy of ISFET measurements using a body effect reduction technique while maintaining constant drain-source voltage and current. With a differential configuration of amplifier circuit, this design technique generates an output signal independent of temperature and long-term drift. In addition, a voltage-controlled DC offset error compensation circuit modulates the extracted signal to the desired DC level for the A/D converter for each sensor. Simulation and experimental results demonstrate the effectiveness of the instrumentation system for monolithic ISFET integration in CMOS technology.

5.1 Body effect in ISFETs

In Complementary MOS (CMOS) technologies, both NMOS and PMOS transistors must be fabricated into the same “local substrate”. In current CMOS processes, the NMOS device is fabricated into a p-type substrate that is why the substrate potential greatly influences the device characteristics. Usually the substrate of NMOS transistors is connected to the most negative supply in the system. Thus, in typical MOS operations the S/D junction diodes must be reverse-biased. It can be proved that with body effect, the threshold voltage is expressed as (5.1) and (5.2):

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) \quad (5.1)$$

$$V_{TH0} = \phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}} \quad (5.2)$$

Where V_{TH0} is the threshold voltage when there is no body effect, ϕ_F is the Fermi potential, γ denotes the body effect coefficient, and V_{SB} is the source-bulk potential difference.

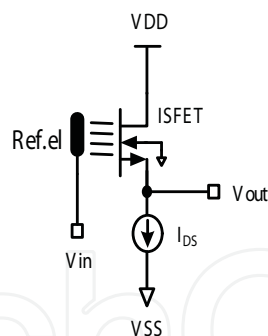


Fig. 18. Source-follower readout circuit of ISFET

Consider the source-follower circuit in Fig. 18. Ignoring the body effect, as the input voltage V_{in} varies, the output voltage V_{out} closely follows the input variation because the drain current remains equal to the I_{DS} . The K_p is device transconductance factor, V_{DS} is drain-source voltage, and $V_{TH}^* = V_{TH} - EPH$ is threshold voltage of ISFET from threshold voltage of FET V_{TH} and from interface potential EPH between sensing membrane and buffer solution.

$$\begin{aligned} I_{DS} &= K_p \left[(V_{GS} - V_{TH}^*) - \frac{V_{DS}}{2} \right] V_{DS} \\ &= K_p \left[(V_{in} - V_{out} - V_{TH}^*) - \frac{V_{DS}}{2} \right] V_{DS} \end{aligned} \quad (5.3)$$

Suppose the substrate is connected to the most negative supply and the body effect is significant in Fig. 18 circuit. As V_{in} increases, V_{out} becomes more positive and the potential difference between the source and the bulk increases. This condition raises the V_{TH} in ISFET. Therefore, the equation (5.3) implies that $V_{in}-V_{out}$ must increase to maintain a constant I_{DS} . Moreover, a non-zero V_{SB} contributes a parasitic change in V_{TH}^* that is not due to variation of ion concentration.

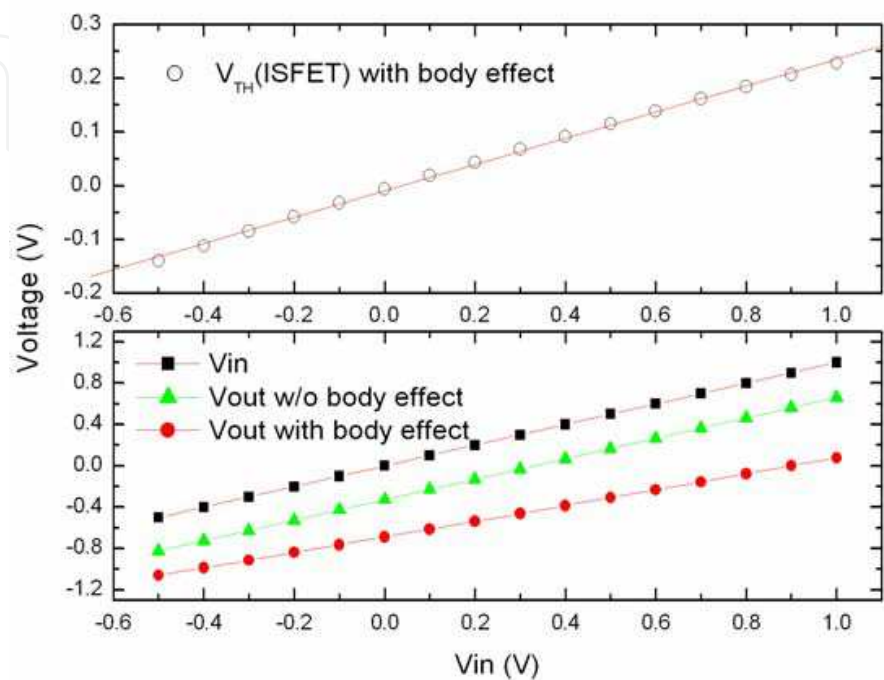


Fig. 19. V_{in} and V_{out} of source-follower readout, with and without (w/o) body effect.

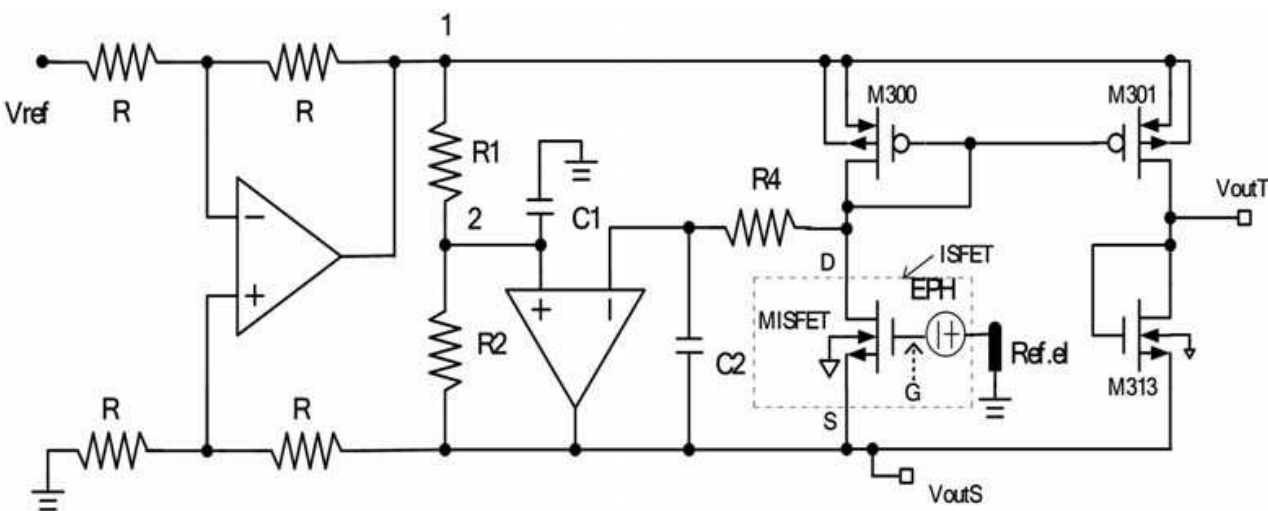


Fig. 20. Schematic diagram of the body-effect reduction readout interface

In order to reduce the body effect in ISFET, the circuitry described in Fig. 5 was modified with a current mirror as shown in Fig. 20. The two devices, MISFET and M313, carry equal drain currents under the influence of body effect (Wade & Tadokoro, 2002). To simplify the analysis, we employ MOSFET in the saturation region. Hence,

$$\begin{aligned}
 I_{DS,misfet} &= I_{DS,m313} \\
 \Rightarrow K_p (V_{GS,misfet} - V_{TH,misfet})^2 &= K_p (V_{GS,m313} - V_{TH,m313})^2
 \end{aligned}
 \quad (5.4)$$

Assume that MISFET and M313 are matched in the same p-type substrate, the extracted signal V_{outT} is equal to the electrolyte-insulator interface potential EPH and is independent of the body effect.

$$\begin{aligned}
 V_{GS,misfet} - V_{GS,m313} &= V_{TH,misfet} - V_{TH,m313} \\
 \Rightarrow -EPH - V_{outS} - (V_{outT} - V_{outS}) & \\
 &= V_{TH0,misfet} + \gamma(\sqrt{2\phi_f + V_{SB,misfet}} - \sqrt{2\phi_f}) - [V_{TH0,m313} + \gamma(\sqrt{2\phi_f + V_{SB,m313}} - \sqrt{2\phi_f})] \\
 \Rightarrow V_{outT} &= -EPH
 \end{aligned}
 \quad (5.5)$$

In general, single ISFET interface circuits do not offer any degree of compensation for temperature dependency or long-term drift. The body-effect reduction readout interface in Fig. 20 accompanies a performance enhancement circuit in Fig. 21. Assume that resistances R are perfectly matched with one another and that op amp have infinite CMRR in the differential amplifier circuit. With V_{outS} and V_{outT} having equal temperature dependency, equal long-term drift as well as common noise, the output signal V_{outU} in (5.6) becomes unaffected by temperature, long-term drift and common noise.

$$V_{outU} = V_{outT} - V_{outS} \quad (5.6)$$

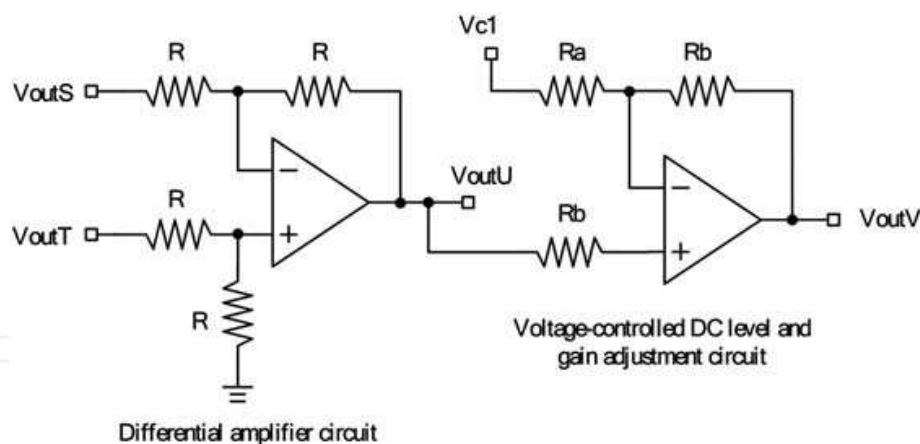


Fig. 21. Differential circuit used for ISFET performance enhancement

In (5.7) is the output signal V_{outV} of voltage-controlled DC offset error compensation and gain adjustment circuit. The first term generates an output signal that is independent from thermal and long-term drift effects, while the second term modulates the extracted signal to the desired DC level for the A/D converter of each sensor.

$$V_{outV} = \left(1 + \frac{R_b}{R_a}\right)V_{outU} - \frac{R_b}{R_a}V_{c1} \quad (5.7)$$

5.2 On-chip circuit implementation and results

A photomicrograph of the realized bridge-type ISFET readout circuit with band-gap reference voltage generator in Fig. 22 was fabricated in Taiwan Semiconductor Manufacturing Company using TSMC 0.35 μm CMOS technology. (BFDSF stands for bridge-type floating drain source follower). The core die size is around $963 \times 892 \mu\text{m}^2$. Fig.23 shows the photomicrograph of the total body-effect reduction and performance enhanced circuitry ($9.1 \times 9.1 \text{ mm}^2$).

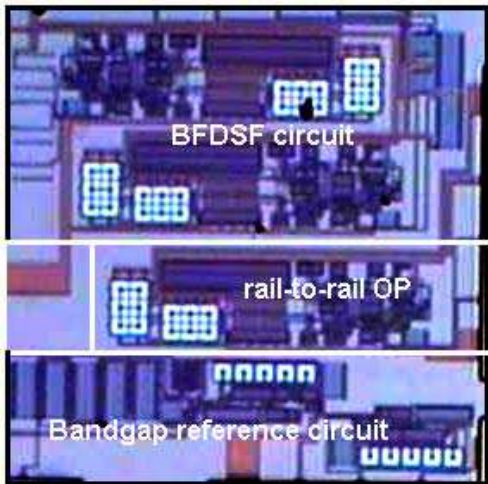


Fig. 22. Photomicrograph of the realized BFDSF circuit ($963 \times 892 \mu\text{m}^2$)

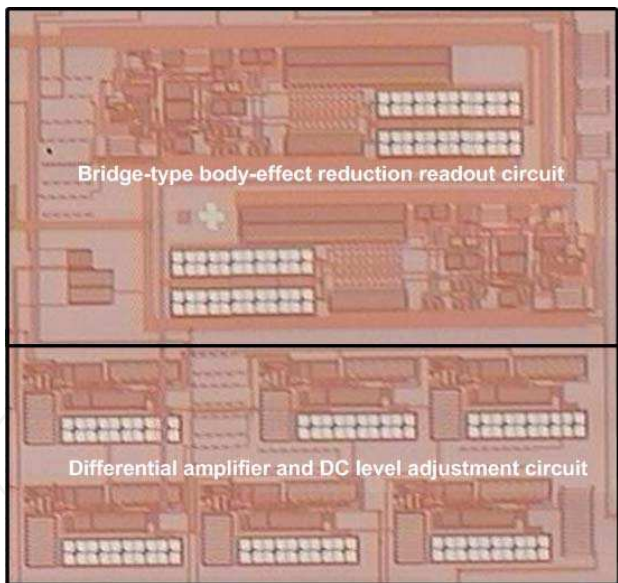


Fig. 23. Photomicrograph of the total body-effect reduction and performance enhanced circuitry ($9.1 \times 9.1 \text{ mm}^2$)

Table 4 depicts the measured bias voltage and current for Al_2O_3 -gate and Si_3N_4 -gate ISFET sensors operated from pH 2 to pH 12. The inaccuracy is only 0.2% in the drain current and only 0.006% in the drain-source voltage, and is attributed to the process variation on circuit resistors. The results show very small variations in the ISFET bias voltage and current and prove that the readout circuit maintains a stable operating point with different pH value and different sensor.

Both	Al ₂ O ₃ ISFET		Si ₃ N ₄ ISFET	
pH	Id s (μ A)	V d s (V)	Id s (μ A)	V d s (V)
2.001	100.2	0.505	100.2	0.505
3.007	100.2	0.505	100.2	0.505
4.007	100.2	0.505	100.2	0.505
5.001	100.2	0.505	100.2	0.505
6.006	100.2	0.505	100.2	0.505
7.006	100.2	0.505	100.2	0.505
8.015	100.2	0.505	100.2	0.506
8.999	100.2	0.505	100.2	0.506
10.035	100.2	0.505	100.2	0.506
11.011	100.2	0.505	100.2	0.506
12.050	100.1	0.505	100.2	0.506

Table 4. Measurement of bias voltage and current for Al₂O₃-gate and Si₃N₄-gate ISFET sensors operating in buffer solutions of different pH

Fig. 24 show the potentials of four terminals in the body-effect reduction circuit over pH range of 2 to 12, namely *VoutS*, *VoutT*, *VoutU* and *VoutV*. Refer to Fig. 20 and Fig. 21. The bulk of ISFET was connected to the most negative supply with *VSS*=-1.65V. The calculated slopes for graphs (a), (b), (c), and (d) are -40.06mV/pH, -48.43mV/pH, -8.22mV/pH and -50.68mV/pH for terminals *VoutS*, *VoutT*, *VoutU* and *VoutV* respectively. The increase of slope for curve (b) compared to curve (a) demonstrates the improvement that resulted from the reduction of body effect. The experimental data presented here correlates well with the simulation data presented in Fig.19.

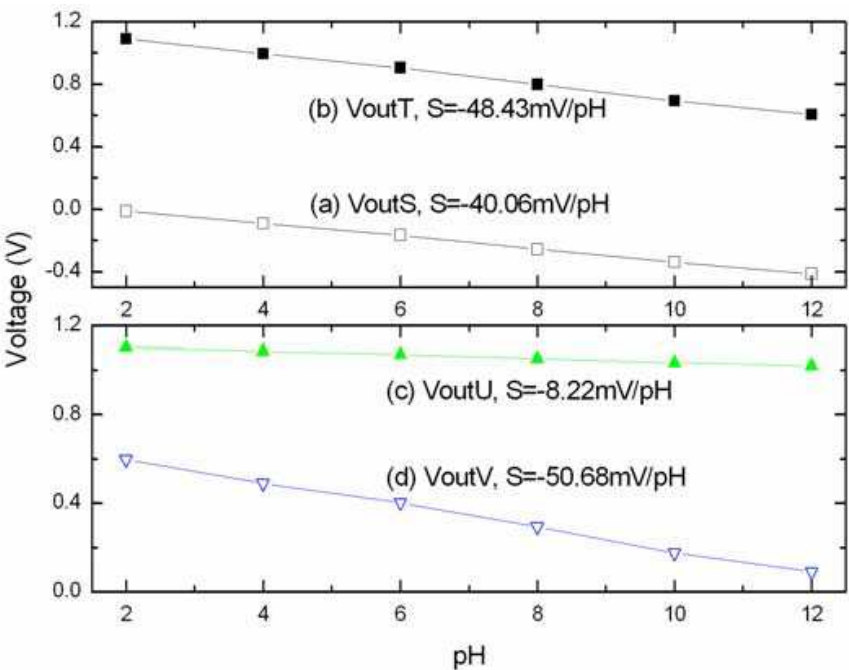


Fig. 24. pH response of ISFET operating in the body-effect reduction circuit with the ISFET bulk connected to *VSS*

5.3 On-board prototyping

Considering the practical applications, Fig. 25 and Fig. 26 give the system diagram and initial prototype of pH meter using separate on-board modules for the readout circuit and the microcontroller unit (MCU). The calibration and measurement routines are coded inside the MPC82G516A MCU. The experimental readings of this pH meter prototype agree with that of commercial ISFET pH meter KS701 (Shindengen Co., Japan) and measures from pH2 to pH12 with 0.1 pH resolution.

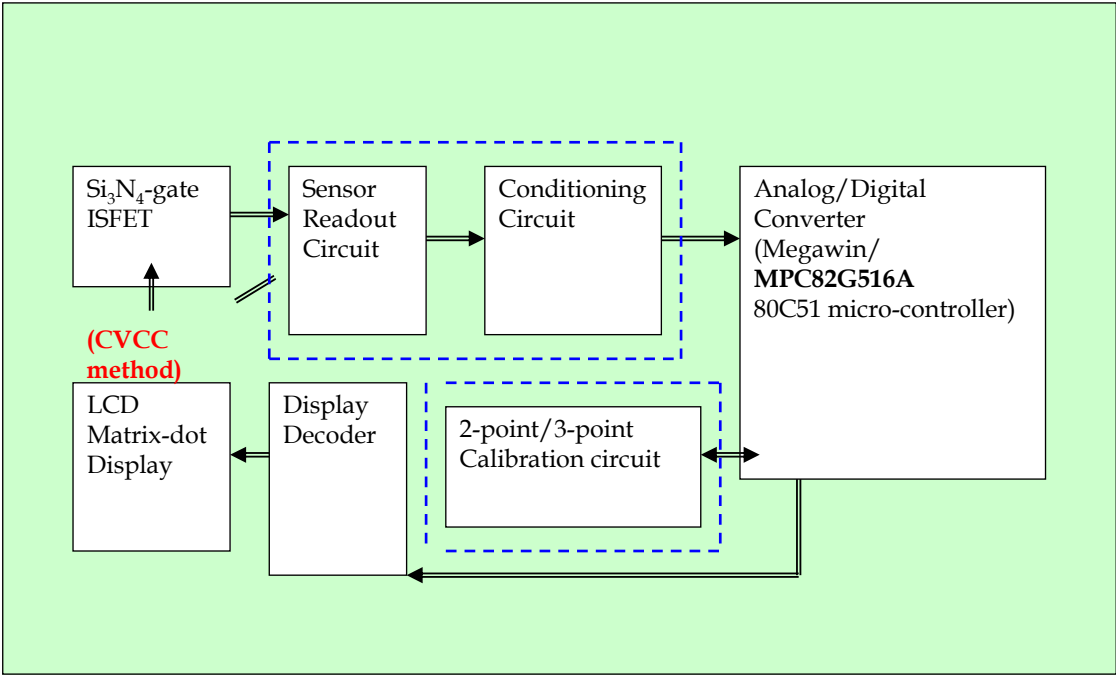


Fig. 25. System block diagram of a prototype of pH meter

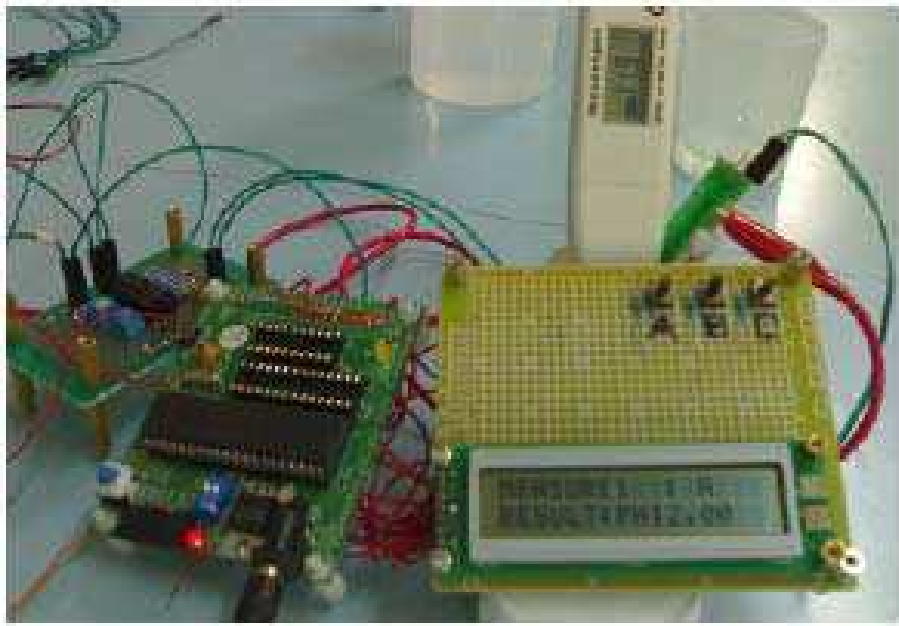


Fig. 26. PCB-based hardware implementation of a pH-meter prototype

6. Conclusion and future works

This chapter explored the characteristics and the non-ideal parameters of ISFET that were important to the practical and long-term sensing applications of ISFET. This chapter also presented series of improved readout circuit techniques that enhanced the performance of ISFET and demonstrated the pH sensing capability of ISFET for environmental monitoring. The SPICE-based drift model of ISFET developed in this chapter can be used for further ISFET-based sensor interface circuit designs. With the advantage of compatible CMOS process and only fewer mask steps, sensor pairs consisting of Si_3N_4 -gate ISFET and depletion-type MOSFET were demonstrated in V_{TH} extractor circuit that provided sensitive measurements with improved temperature compensation. In addition, the proposed ISFET bridge-type CVCC circuitry with body-effect reduction technique not only enhanced the noise rejection performance but also removed the interferences from source and drain terminals.

For future works, the multi-ion sensing based on ISFET sensor arrays and their corresponding signal processing algorithms such as independent component analysis or blind source separation will be continuously studied. In addition, the integrated sensors in a standard CMOS process will be further investigated for diversified field applications.

In conclusion, CMOS technology and circuitry play more important roles on biosensor applications especially in the field of sensor interface design and development. The response of biosensor can be potential, current and impedance changes. Thus, the systematic and hierarchical approaches to develop more advanced electronic tongue using potentiometric, amperometric or impedimetric readout circuit techniques should be emphasized through the collaboration among academic, industrial and research organizations over the world.

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8. References

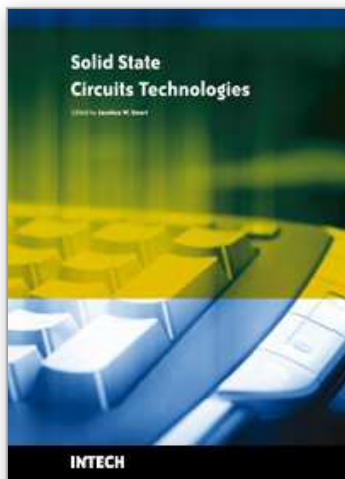
- Bausells, J.; Carrabina, J.; Errachid, A.; Merlos, A. (1999) Ion-sensitive field effect transistors fabricated in a commercial CMOS technology, *Sensors and Actuators B*, Vol. 57, 1999 56-62
- Bergveld, P. (1970). Development of an ion sensitive solid-state device for neurophysiological measurement, *IEEE Trans. Biomed. Eng.*, Vol. 17, 1970, 70-71
- Bergveld, P. (1991). Future applications of ISFETs, *Sensors and Actuators B*, Vol. 4, 1990, 125-133
- Bergveld, P. (2003). Thirty years of ISFETOLOGY-What happened in the past 30 years and what may happen in the next 30 years, *Sensors and Actuators B*, Vol. 88, 2003, 1-20

- Bousse, L.; Hafeman, D.; Tran, N. (1990). Time-dependence of the chemical response of silicon nitride surface, *Sensors and Actuators B*, Vol. 1, 1990, 361-367
- Chin, Y.; Chou, J.; Sun, T.; Chung, W.; Hsiung, S. (2001). A novel pH sensitive ISFET with on chip temperature sensing using CMOS standard process, *Sensors and Actuators B*, Vol. 76, 2001, 582-593
- Chou, J. & Hsiao, C. (2000). Drift behavior of ISFETs with a-Si: H-SiO₂ gate insulator, *Materials Chemistry and Physics*, Vol. 63, 2000, 270-273
- Chung, W.; Yang, C.; Pijanowska, G.; Krzyskow, A. (2004). ISFET interface circuit embedded with noise rejection capability, *Electronics Letters*, Vol. 40, 2004, 1115-1116
- Chung, W.; Chang, K.; Hong, D.; Cheng, C.; Cruz, F.; Liu, T.; Yang, C.; Chiang, J.; Pijanowska, G.; Dawgul, M.; Torbicz, W.; Grabiec, P.; Jarosewicz, B. (2008). An electronic tongue system design using ion sensitive field effect transistors and their interfacing circuit techniques, *Proceedings of the 17th Biennial University/Government /Industry Micro-Nano Symposium*, pp. 44-48, ISBN, 978-1-4244-2484-9, Louisville, KY, USA, July, 2008, IEEE, Louisville, KY
- Ciosek, P. & Wroblewski, W. (2007). Sensor array for liquid sensing – electronic tongue systems, *Analyst*, Vol. 132, 2007, 963-978
- Garde, A.; Alderman, J. & Lane, W. (1995). Development of a pH-sensitive ISFET suitable for fabrication in a volume production environment, *Sensors and Actuators B*, Vol. 27, 1995, 341-344
- Jamasb, S.; Collins, S.; Smith, R. (2000). A physical model for drift in pH ISFETs, *Sensors and Actuators B*, Vol. 49, 2000, 146-155
- Kuhnhold, R. & Ryssel, H. (2000). Modeling the pH response of silicon nitride ISFET devices, *Sensors and Actuators B*, Vol. 68, 2000, 307-312
- Lauwers, E.; Suls, J.; Gumbrecht, W.; Maes, D.; Gielen, G.; Sansen, W. (2001). A CMOS multiparameter biochemical microsensor with temperature control and signal interfacing, *IEEE J. Solid State Circuits*, Vol. 36, 2001, 2030-2038
- Liao, H. (2000). Novel calibration and compensation technique of circuit design for Biosensor, *Master Thesis*, Chung Yuan Christian University, Chung-Li, Taiwan, 2000.
- Martinoia, S.; Lorenzelli, L.; Massobrio, G.; Margesin, B.; Lui, A. (1999) A CAD system for developing chemical sensor-based microsystems with an ISFET-CMOS compatible technology, *Sensors and Materials*, Vol. 11, 1999, 32-49
- Martinoia, S. & Massobrio, G. (2000). A behavioral macromodel of the ISFET in SPICE, *Sensors and Actuators B*, Vol. 62, 2000, 182-189.
- Morgenshtein, A.; Sudakov-Boreysa, L.; Dinnar, U.; Jakobson, C.; Nemirovsky, Y. (2004) CMOS readout circuitry for ISFET microsystems, *Sensors and Actuators B*, Vol. 97, 2004, 122-131
- Palan, B.; Santos, F.; Courtois, B.; Husak, M.; (1999) Fundamental noise limits of ISFET-based microsystems, *Euroensors*, Vol. 13, 1999, 169-172
- Ravazzi, L. & Conci, P. (1998) ISFET sensor coupled with CMOS read-out circuit microsystem, *Electron Letters*, Vol. 34, 1998, 2234-2235
- Wada, K. & Tadokoro, Y. (2002) Design of a body-effect reduced-source follower and its application to linearization technique, *Proceedings of IEEE Int. Symposium on Circuits and Systems*, Vol. 3, 2002, 723-726

- Wong, H. & White, H. (1989) A CMOS -integrated ISFET operational amplifier, chemical sensor employing differential sensing, *IEEE Trans. Electron Devices*, Vol. 36, 1989 479-487
- Yin, L.; Chou, J.; Chung, W. ; Sun, T. ; Hsiung, S. (2001). Study of indium tin oxide thin film for separate extended gate ISFET, *Materials Chemistry and Physics*, Vol. 70, 2001, 12-16

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